REMARKS

The present Amendment amends claims 1 and 15, and leaves claims 2-14 and 16-19 unchanged. Therefore, the present application has pending claims 1-19.

Applicant's attorney, the undersigned wishes to thank Primary Examiner Truong, the Primary Examiner who signed the July 12, 2007 Office Action, for the courtesy extended during the interview of October 25, 2007. As discussed during the interview Applicant is very concerned with the examination of this application in light of the various incorrect allegations made by the Examiner throughout the prosecution of this application that have not been changed or reconsidered in light of clear evidence that the allegations were incorrect. Accordingly as discussed during the interview Applicant, by way of the undersigned, requests close scrutiny of the examination of this case particularly any allegations to be made in the forthcoming Office Action responding to the present response.

Primary Examiner Truong and The Examiner are strongly urged to contact the undersigned by telephone so as to discuss any further outstanding issues of the present application prior to issuing the forthcoming Office Action.

Claims 1-19 stand rejected under 35 USC §103(a) as being unpatentable over Martin (U.S. Patent No. 5,504,873) in view of Akizawa (U.S. Patent No. 5,548,724) and further in view of Abe (U.S. Patent No. 6,880,104). This rejection is traversed for the following reasons. Applicants submit that the features of the present invention as now more clearly recited in claims 1-19 are not taught or suggested by Martin, Akizawa or Abe whether taken individually or in combination with each other as suggested by the

Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Independent claims 1 and 15, from which the remaining claims depend, clearly recite that the present invention provides a storage device system and a method of activating a storage device system, wherein the storage device system includes a plurality of storage devices in which information is stored, a storage device control section for controlling storage of information in the storage devices, a connection unit connected to the storage device control section and first and second processors.

According to the present invention the first processor is connected to a local area network (LAN) external to the storage device system and converts data of a file access form received over the LAN into data of a block access form.

Further, according to the present invention the second processor is connected to the storage device control section via the connection unit and accesses the storage devices via the connection unit and the storage device control section in response to data of the block access form issued from the first processor.

Particularly, according to the present invention as now more clearly recited in the claims the second processor controls activation of the first processor including resetting the first processor by the second processor, wherein the resetting of the first processor by the second processor includes stopping supplying power to the first processor, re-supplying power to the first processor and activating a Basic Input/Output System (BIOS) of the first processor.

The above described features of the present invention clearly recited in the claims are illustrated, for example, in Fig. 17 and described in the corresponding portions of the specification.

The above described features of the present invention clearly recited in the claims are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention as now more clearly recited in the claims are not taught or suggested by Martin, Akizawa or Abe whether taken individually or in combination with each other as suggested by the Examiner.

In the Office Action the Examiner incorrectly alleges that the control processor 114 of Martin corresponds to the first processor as recited in the claims. Further, the Examiner incorrectly alleges that the control processor 114 of Martin is connected to a local area network (LAN) external to the storage system 10 via signal lines 95 and 80 the same as the first processor recited in the claims.

It is abundantly clear that the Examiner has completely mis-described the teachings of Martin in a failed attempt to support her allegations that Martin teaches features corresponding to the features recited in the claims.

For example, signal line 95 as taught by Martin is not a LAN nor is it connected to a LAN external of the storage system 10 as recited in the claims. Signal line 95 as taught by Martin connects the control processor 114 to each of the IFS computers 19, 14, 16, and 18. The control processor 114 and the IFS computers 19, 14, 16, and 18 are clearly internal of the storage system

10. Element 80 is simply a disk device included in each the IFS computers 19, 14, 16, and 18.

It appears the Examiner is confused as to what Fig. 2A of Martin represents. Fig. 2A of Martin simply illustrates the internal details of each of the elements included in the storage system 10 as illustrated in Fig. 1. Thus, all of the elements illustrated in Fig. 2A of Martin are internal of the storage system 10.

Thus, when Fig. 2A is properly viewed, the control processor 114 as taught by Martin forms a part of the control subsystem 40 which is not connected to a LAN external to the storage system, nor does it receive data on a LAN external to the storage system from a host computer to be stored in the storage devices included in the storage system, nor does it perform a conversion of the data received from the host computer on a LAN external to the storage system so as to convert data of the file access form into data of the block access form which is stored in the storage devices as recited in the claims.

Martin teaches in col. 4, lines 48-59 thereof that:

> "The control subsystem 40 allocates and de-allocates the common resources present in the mass storage library system 10. When an interface tape server computer 14, 16 or 18 or the interface disk server computer 19 receives a command to read or write data, it first requests resources (i.e., files or volumes) from the control subsystem computer 40 which will then initialize and position the appropriate resources and inform the requesting IFS of resource availability. Control of the recorder resources is then passed to the requesting IFS. Once the operation is complete, the controlling IFS notifies the control computer 40 and the resources are de-allocated."

Thus, as is clear from the above the control processor 114 is not connected in the same manner, nor does it perform the same or similar functions, as the first processor as recited in the claims completely contrary to the allegations by the Examiner.

In the Office Action the Examiner incorrectly alleges that the console processor 116 of Martin corresponds to the second processor as recited in the claims. In addition the Examiner incorrectly alleges that the console processor 116 of Martin is connected to the storage device control section via a connection unit 110. Further, the Examiner incorrectly alleges that the console processor 116 accesses the storage devices via the connection unit 110 and the storage control section in response to data of the block access form from the first processor and that the console processor 116 controls activation of the first processor.

Again it is abundantly clear that the Examiner has completely mis-described the teachings of Martin in another failed attempt to support her allegations that Martin teaches features corresponding to the features recited in the claims.

For example, the console processor 116 as taught by Martin is included as part of the control subsystem 40 described above. Although the console processor 116 is shown in Martin as being connected to the control processor 114 via a signal line 110, there is absolutely no teaching or suggestion in Martin that data is exchanged between the control processor 114 and the console processor 116 similar to that of the first and second processors as recited in the claims. More particularly, there is no teaching or suggestion in Martin that the console processor receives converted data of

the block access form from the control processor 114 from external of the storage system, that the converted data of the block access form was converted from data of the file access form, and that the converted data of the block access form is stored in the storage devices as recited in the claims. The Examiner seems not to understand this feature nor has the Examiner properly addressed these features in the claims.

Further, in the Office Action the Examiner incorrectly alleges that the console processor 116 of Martin controls activation of the control processor 114 including resetting the control processor 114 by the console processor 116, re-supplying power to the control processor 114 and activating a Basic Input/Output System (BIOS) of the control processor 114 as in the present invention as recited in the claims. It should be noted that the claims now recite that the resetting of the first processor by the second processor includes stopping supplying power to the first processor, re-supplying power to the first processor and activating a Basic Input/Output System (BIOS) of the first processor. Such features are also not taught or suggested by Martin.

The above noted allegation by the Examiner is simply false. The passages in Martin referred to by the Examiner in the Office Action to support the above noted allegation do not provide any support whatsoever. In fact the passages in Martin referred to by the Examiner in the Office Action teach away from the features recited in the claims.

Applicant again emphasizes that one basic factor the Examiner has failed to address is how the control processor 114 and console processor 116 as taught by Martin are equivalent to the first and second processors as recited in the claims. The claims clearly recite that the first processor receives

data of a file access form from the host computer on a LAN external of the storage system and converts the data of the file access form to data of a block access form and the second processor receives the data of the block access form and transfers the data to the disk drive. The control processor 114 and console processor 116 as taught by Martin form a part of the control subsystem 40 which "allocates and de-allocates the common resources present in the mass storage library system 10. In other words the control processor 114 and console processor 116 as taught by Martin operate together to control the operations of the IFS computers 19, 14, 16, and 18, the switch module 42, the drive unit 44 and the transport system 56. There is absolute no teaching, suggestion or even disclosure in Martin that the control processor 114 and console processor 116 are equivalent to the first and second processors as recited in the claims.

Further, according to the present invention the first and second processors as recited in the claims perform processings with respect to file access type data and block access type data. The Examiner has not shown where such teaching can be found in Martin besides the incomplete allegation that a conversion process is performed in Martin. Those of ordinary skill in the art clearly understand that a file access or file access type data is quite different from a block access of block access type data. Thus, the first processor performs functions in the handling of data differently than the second processor and a conversion is performed between the two different types of data according to the present invention.

There is no similar teaching in Martin. In Martin, the control processor 114 and console processor 116 merely perform the control of allocations of

resources as described in col. 4, lines 48-59. There is absolutely no teaching or suggestion in Martin that one of the control processor 114 and console processor 116 performs processing according to file access type data and that the other of the control processor 114 and console processor 116 performs functions according to block access type data as in the present invention.

Thus based on all of the above, Martin fails to teach or suggest a first processor that is connected to a local area network (LAN) external to said storage device system, that converts data of a file access form received over said LAN into data of a block access form as recited in the claims.

Further, Martin fails to teach or suggest a second processor that is connected to said storage device control section via said connection unit, that accesses said plurality of storage devices via said connection unit and said storage device control section in response to data of the block access form issued from said first processor, and that controls activation of said first processor including resetting said first processor by said second processor, wherein the resetting of the first processor by the second processor includes stopping supplying power to the first processor, re-supplying power to the first processor and activating a Basic Input/Output System (BIOS) of the first processor as recited in the claims.

The above described deficiencies of Martin are not supplied by Akizawa. Akizawa is merely relied upon by the Examiner for an alleged teaching of converting information of a first form received over the external network into information of a second form. However, at no point is there any teaching or suggestion in Akizawa of the above described features of the

present invention now more clearly recited in the claims that are not taught or suggested by Martin. More particularly Akizawa does not teach or suggest the conversion of file access type data to block access type data as recited in the claims.

The above described deficiencies of both Martin and Akizawa are not supplied by Abe. Abe merely discloses that a memory protection unit obtains control of a DIMM 31 from a chip set by way of switching switches 11 and 12 when detecting an unexpected power shutdown. Abe is completely silent as to the activation of a NAS processor, in other words a processor included in a storage system that as recited in the claims.

In the Office Action the Examiner attempts to equate the memory protection unit 10 of Abe to the second processor (i.e. I/O processor) as recited in the claims. However, the memory protection unit 10 of Abe is quite different from I/O processor of the present invention as recited in the claims. The I/O processor of the present invention as recited in the claims performs accessing of storage devices in response to data in block access form received from the NAS processor. Such features are clearly and absolutely not taught or suggested by Abe.

Thus, Martin, Akizawa and Abe all suffer from the same deficiencies relative to the features of the present invention as now more clearly recited in the claims. Therefore, combining Martin, Akizawa and Abe in the manner suggested by the Examiner in the Office Action does not render obvious the claimed invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 USC §103(a) rejections of claims 1-

19 as being unpatentable over Martin in view of one or more of Akizawa and Abe is respectfully requested.

The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 1-19.

In view of the foregoing amendments and remarks, applicants submit that claims 1-19 are in condition for allowance. Accordingly, early allowance of claims 1-19 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (TMI-5010).

Respectfully submitted,

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